A Compact Active Filter to Eliminate Common-Mode Voltage in SVPWM Electric Motor Drives

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Dedication

To my friends and family

Abstract

This thesis presents an active compensation device for common-mode (CM) voltage elimination in 3-phase space-vector pulse-width-modulated (SVPWM) inverters. The proposed device consists of a single-phase 2-level inverter in the form of an H-bridge which supplies a compensating voltage to the inverter via a step-up common-mode transformer tied to all 3 phases at the output. The H-bridge active filter is supplied by a low voltage bus and switched several orders of magnitude faster than the inverter switching frequency. This device takes advantage of the direct knowledge of the switching pulses sent to the inverter to predict and generate the compensating voltage. A technique is employed to subtract the low frequency harmonics from the modulation of the H-bridge which allows for the size of the common-mode transformer to be reduced significantly. Additional passive filter components are added to produce an effective compensating voltage. This thesis will review existing common-mode voltage compensation techniques and demonstrate that the proposed method is a logical choice for certain drive applications. Design considerations are included to provide understanding and guidance for hardware implementation of the device, as well as MATLAB/Simulink simulation results to demonstrate the operation of the active compensation device. Final validation is presented through experimental results from a hardware prototype.

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Chapter 1

Introduction

1.1 Motivation

It is well known that the use of pulse width modulated (PWM) power electronic motor drives leads to a common mode (CM) voltage seen at the motor terminals [1, 2, 3, 4, 5, 6, 7, 8, 9, 10]. This CM voltage occurs at the switching frequency of the inverter, and results in voltage buildup on the motor shaft due to capacitive coupling. Several harmful effects can result from this shaft voltage buildup, most notably currents and which pass through the motor bearings and significantly reduce their lifetime [10]. Wide band gap (WBG) devices such as Silicon Carbide (SiC) MOSFETs are able to switch at higher frequencies at comparable voltage ratings to silicon devices, and likewise higher voltages at comparable switching frequencies [11]. These properties, though advantageous in many aspects to inverter operation, increase stress on the motor due to escalated dV/dt of the CM voltage and more frequent occurrence of CM voltage transitions. With the emergence of WBG devices and their expected popularity for use in variable frequency motor drives, the need for developing an effective and practical CMV mitigation technique is pronounced more than ever.

Various passive and active techniques have been proposed and/or implemented for PWM motor drives to eliminate/mitigate CM voltage [12, 13, 14, 15, 16, 17, 18, 19, 20]. Passive output filters have been widely used with varying levels of success. These filters are often bulky in size and expense, and their design process can be complex, consisting of a trial-and-error process in order to provide adequate filtering without

costly side-effects [12]. Open-end winding dual-VSI configurations have been shown to significantly remove CM voltage, but require an additional inverter rated for the full load [13, 14, 15]. Active methods focused on supplying an equal and opposite CM voltage to all three phases via a four-winding common mode transformer have been reported in several variations [17, 16, 18, 19, 20]. Proposed in [17] and further improved in [20], an active compensation device composed of push-pull transistors and voltage-sensing circuit, successfully reduced the ground current and conducted EMI from common mode voltage. This method has proven difficult to implement above certain voltage levels because of the lack of available devices at needed voltage and current ratings. In [19], a single-leg, four-level inverter is used in simulation in place of push-pull transistors in order to produce the necessary compensating voltage. Pairodamonchai [18] used this method in experimentation with the addition of passive elements to further filter the output CM voltage and reduce the physical size of the common-mode transformer.

1.2 Thesis Contribution

This thesis proposes a new approach to actively filtering CM voltage that overcomes several of the shortcomings in previous CM voltage mitigation techniques. This new method utilizes a 2-level PWM H-bridge inverter to supply a compensating voltage via a 4-winding step-up CM transformer. Design constraints as well as a new technique for removing the lower-order harmonics of the compensating voltage are described. Transient and spectra analysis from MATLAB/Simulink simulation results are used to verify the performance of the proposed active filter device. Experimental results from a hardware prototype act as a proof of concept for this new filter, and future results will aim to compare the effectiveness of this new device to conventional techniques explored in a previous investigation on CM voltage mitigation in a motor drive system utilizing SiC MOSFETs.

- Chapter 2 briefly presents a background of common-mode voltage and it's harmful effects in PWM motor drives
- In Chapter 3 the proposed active filter design is outlined
- Chapter 4 presents simulation results of the proposed filter

- In Chapter 5 hardware results are presented and analyzed
- Chapter 6 concludes the thesis and comments on future work

Note: Portions of the material presented in this thesis have been submitted for publication in [21]

Chapter 2

CMV in PWM Motor Drives

2.1 Common-Mode Voltage Background

As mentioned previously, an undesirable byproduct the use of pule-width modulated (PWM) inverters is the common mode voltage at the output of the inverter that is seen at the motor input terminals. The source of this common-mode voltage for a conventional 3-phase, 2-level voltage source inverter (VSI) will now be discussed.

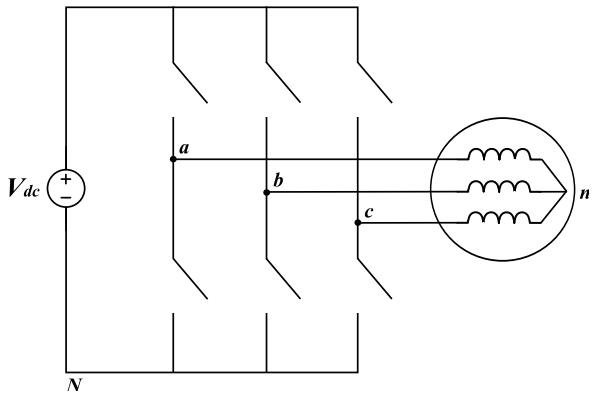

Figure 2.1: Conventional 3-phase 2-level Voltage Source Inverter

As can be seen in Fig.2.1, at any instant of time, depending on the orientation of the switches in each of the three phases of the inverter, a voltage of either V_{DC} or 0 appears at the output terminals of the inverter phases. The common-mode voltage that is present at this instant of time with respect to the negative of the DC bus (N

in Fig.2.1) is equal to the sum of the three phase-to-neutral voltages divided by the number of phases, or:

$$V_{CM} = \frac{V_{aN} + V_{bN} + V_{cN}}{3} \tag{2.1}$$

The common-mode voltage in this paper will be referred to with respect to the mid-point of the DC bus. This gives us the following equation for the value of the common-mode voltage at any instant of time:

$$V_{CM} = \frac{V_{aN} + V_{bN} + V_{cN}}{3} - \frac{V_{DC}}{2} \tag{2.2}$$

Table 2.1 below gives the value of the common-mode voltage based on the orientation of each of the single-phase legs of the inverter. A switch orientation of 1 refers to the top switch in the leg being 'on' (bottom being 'off') and therefore a voltage of V_{DC} appearing at the output. Likewise, a switch orientation of 0 refers to the top switch in the leg being 'off' (bottom being 'on') and therefore a voltage of 0 appearing at the output.

Table 2.1: V_{CM} based on Inverter Switch Orientation

Switch Orientation			Common-Mode Voltage
Sa	Sb	Sc	V_{CM}
0	0	0	$-V_{DC}/2$
1	0	0	$-V_{DC}/6$
0	1	0	$-V_{DC}/6$
0	0	1	$-V_{DC}/6$
1	1	0	$V_{DC}/6$
1	0	1	$V_{DC}/6$
0	1	1	$V_{DC}/6$
1	1	1	$V_{DC}/2$

It can be seen in Table 2.1 that for the eight available switch orientations of a 3-phase, 2-level VSI, there are four different levels of common-mode voltage. These levels

are $\pm V_{DC}/2$, and $\pm V_{DC}/6$ with respect to the mid-point of the VSI's DC bus.

The inverter modeled and used in this research utilizes space-vector pulse-width-modulation (SVPWM) as it's control algorithm. In SVPWM, the position of the voltage space-vector determines which state vectors are being utilized during that switching interval. Each state vector, as shown in Fig. 2.2) below, represents one of each of the 3-phase switching orientations, where each state uses the notation $[Sa\ Sb\ Sc]$ to note the orientation of the switches in each phase. Not shown in the figure are the two zero vectors, [0 0 0] and [1 1 1], which represent the state when all phase legs are driven 'low' and all phase legs are driven 'high' respectively.

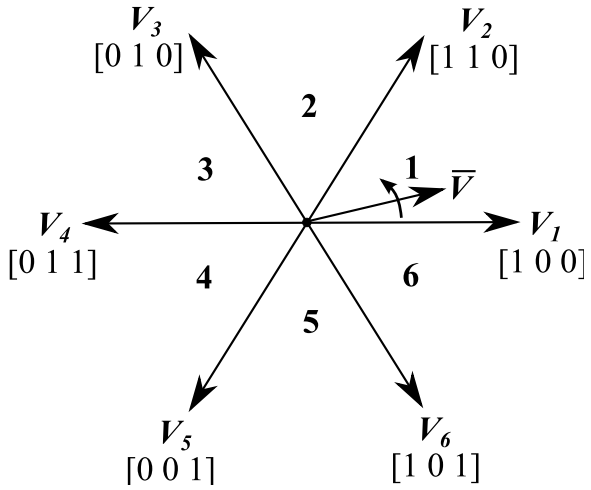

Figure 2.2: State vectors of SVPWM

For commonly-used carrier-based SVPWM, based on the position (sector) of the voltage space-vector $\bar{V}$, the inverter cycles through the two adjacent state vectors and the two zero vectors during one switching time period. For example, the modulation scheme during one switching cycle for a voltage space-vector in sector 1 would follow the pattern shown in Table 2.2 below. The inverter progresses through state vectors from left to right (V_0 and V_7 represent the zero vectors [0 0 0] and [1 1 1] respectively). The amount of time the inverter stays in each state is dependent upon the position of the voltage space-vector that is to be synthesized at that instant in time.

Table 2.2: VSI Modulation Scheme for Space-Vector in Sector 1

State Vector							
V_0	V_1	V_2	V_7	V_7	V_2	V_1	V_0

Figure 2.3 gives a visual representation of the progression of switching states and the resulting common-mode voltage that is developed.

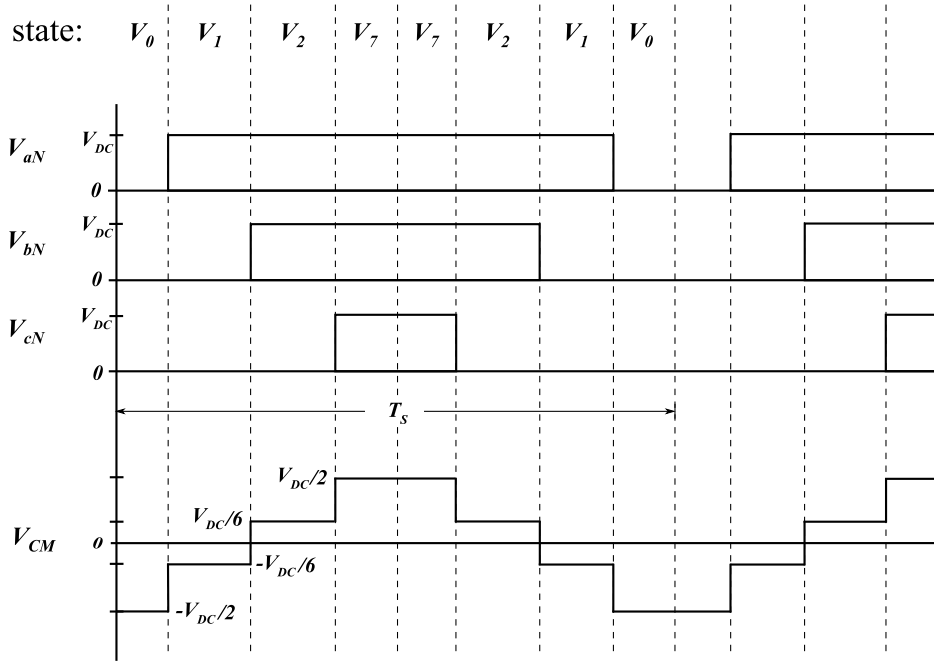

Figure 2.3: SVPWM phase voltages and V_{CM} over one switching time period

The common-mode voltage waveform that is developed is a four-level waveform with a peak-to-peak voltage of V_{DC}, the inverter DC-bus voltage. V_{CM} repeats itself once every switching time period T_s, and therefore occurs at the switching frequency of the inverter. Furthermore, there are six step-transitions in each switching time period with

the rate of change of each step being that of the individual switches in the inverter.

2.2 Shaft Voltage Buildup and Bearing Currents

Research has shown in the past the undesirable and harmful effects that common-mode voltage can have on induction motors driven by pulse-width-modulated power electronic inverters, and how to accurately model these systems [1, 2, 3, 4, 5, 6, 7, 8, 9, 10]. In its most simplified sense, a capacitive coupling between the rotor shaft and ground provides a mechanism for the buildup of shaft voltage when excited by a common-mode (zero-sequence) voltage provided by the PWM inverter [22]. A resulting bearing current will flow from the shaft through the bearings to ground that is determined by the impedance characteristic of the bearings [10]. Along with electrostatically induced induced bearing currents caused by the dV/dt of the common-mode voltage, the shaft voltage can cause so-called electric discharge machining (EDM), where a breakdown of the lubricant between the bearing and case leads to a discharge event through the bearing. Bearing currents in general are undesirable as they signify losses in the system without providing any useful torque, but more importantly, they can cause damage or even failure to the bearing themselves [4]. Large enough shaft voltages and resulting bearing currents have been shown to significantly reduce the lifetime of motor bearings in adjustable speed power electronic based drives.

2.3 Wide Band Gap Devices

Recent advances and declining costs of wide band gap (WBG) power semiconductor devices, made from materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN), has led to increased interest in the implementation of such devices in everyday power electronic applications. Further decreases in cost are likely to lead to increased production and implementation in variable frequency drives in the near future. Among the advantages of WBG devices is the ability to switch at much higher voltage levels for comparable switching frequencies, or likewise, much higher switching frequencies at comparable voltage levels. With these added benefits, though, come magnified negative effects as it relates to common-mode voltage and bearings currents. Larger relative

bus voltages in inverters switching at comparable frequencies means higher dV/dt stress, and faster relative switching frequencies lead to these voltage transitions occurring more often, all of which lead to increased EMI and therefore bearing damage. Recent studies have shown these magnified effects experimentally.

Chapter 3

Proposed Active Filter

3.1 Filter Design

Using the notion of injecting an equal and opposite voltage via a common-mode transformer between the output of the inverter and the motor terminals, several design changes and improvements were made to previous active compensation methods and are detailed in this section. The proposed method uses an active filter composed of a 2-level pulse width modulated H-bridge connected to a step-up common mode transformer. A block diagram of the full system schematic is shown in Fig. 3.1. The H-bridge active filter is switched orders of magnitude faster than the inverter is being switched, so that each voltage level of the CM voltage profile can be matched, as is possible with PWM. Wye-connected filter capacitors are added to the output after the active filter to further attenuate the CM voltage seen at the motor terminals. Shown in the common-mode equivalent circuit of Fig. 3.3, the filter capacitor works in combination with the primary and secondary-side leakage inductances and winding resistances to filter out the higher frequency switching of the voltage supplied by the H-bridge.

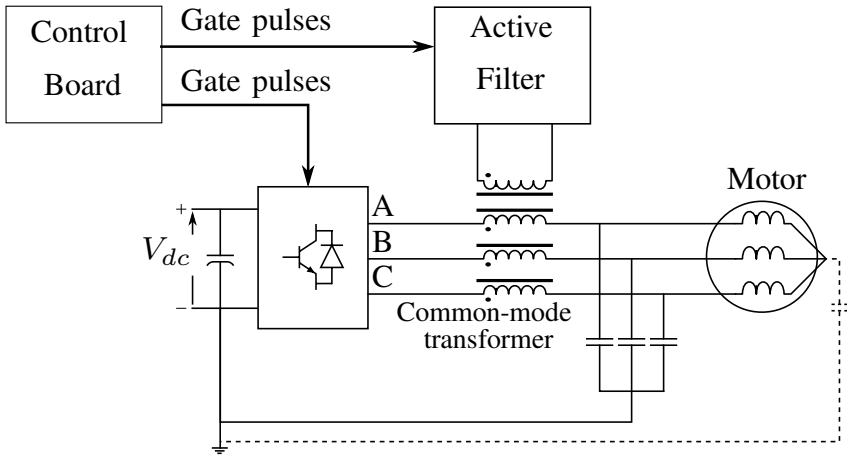

Figure 3.1: Full proposed active filter diagram

There are distinct advantages to the method being proposed here, as follows:

- The voltage produced by the H-bridge is directly controlled based on the gate pulses being sent to the inverter, therefore there is no sensing network needed to measure the CM voltage level at any given instant. This reduces the hardware cost and size requirements and also removes any delay time in the production of the compensating voltage relative to the CM voltage of the inverter.

- Unlike the approaches using a single-leg four-level inverter, PWM is used to obtain each of the four levels of the CM voltage. This means that there is no need to actively balance voltages across a network of capacitors.

- The proposed PWM technique eliminates passive circuit components found in the single-leg four-level approaches to prevent the active filter from suppressing low-frequency CM voltage (explained in more detail below).

- The use of a step-up common-mode transformer allows for the size and voltage rating of the switches in the H-bridge to be lower, since they will no longer be subject to the full DC bus of the inverter. This means that less expensive devices can be used and that they can be operated at faster switching frequencies with lower losses as compared to previously referenced methods.

Since the H-bridge is designed to use a lower voltage DC bus than the VSI, a separate voltage source is needed, which adds additional hardware. However, this is not viewed as a major drawback since the DC bus does not need to be isolated from the VSI's dc bus and the current requirements are expected to be very low, meaning that the dc bus can be easily obtained through simple supporting circuitry such as commercially available prepackaged buck converters or linear regulators.

3.2 CM Equivalent Circuit

Starting with a full circuit schematic for the 3-phase motor inverter with added active filter and attached induction motor, a common-mode equivalent circuit was derived. This equivalent circuit was used in order to make design decisions for the active filter, common-mode transformer, and additional filter components.

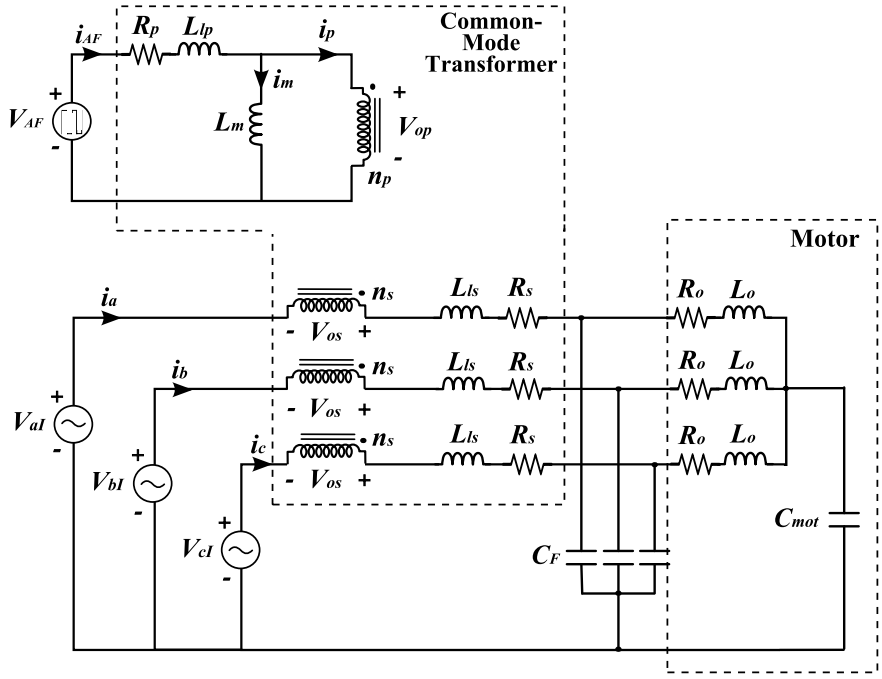

Figure 3.2: Full 3-phase circuit

Fig. 3.2 depicts the full 3-phase equivalent circuit. V_{AF} represents the output voltage

of the active filter H-bridge, and is shown tied to each of the inverter phases via a 4-winding common-mode transformer. The standard simplified model of a transformer is used to represent the winding resistances and leakage inductances of the primary and secondary windings as well as the magnetizing inductance. The induction motor is modeled as a 3-phase RL load with its neutral point coupled to ground by a capacitance. As mentioned previously, an additional wye-connected filter capacitor is added from the three phases to ground in order to provide additional filtering properties.

From the full 3-phase circuit, we can derive the following common-mode equivalent circuit:

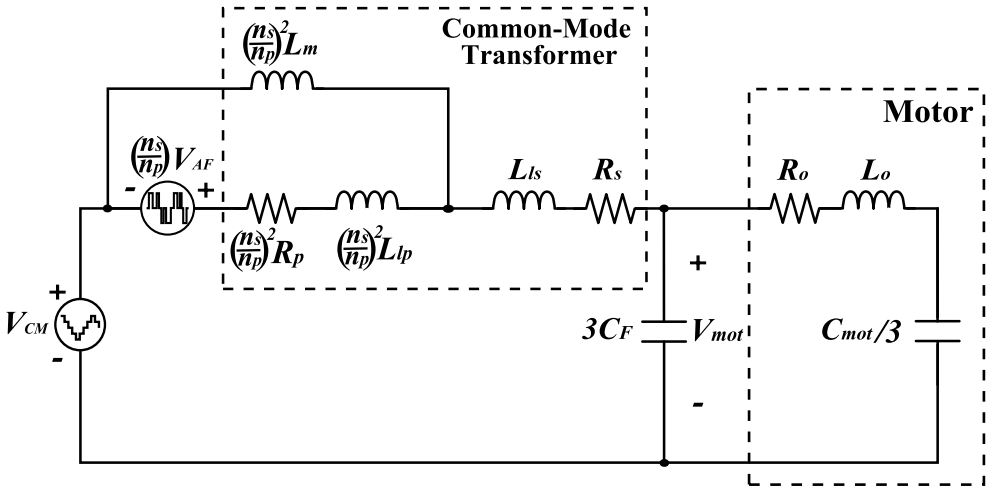

Figure 3.3: Common mode equivalent circuit

As seen in Fig. 3.3, V_{CM} represents the incident common-mode voltage produced at the output of the inverter. V_{AF}, the PWM voltage supplied by the active filter H-bridge, is scaled by the CM transformer duty ratio (n_s/n_p). Another advantageous characteristic of the step-up common-mode transformer proposed is that the magnetizing and primary-side leakage inductances (L_m and L_{lp} respectively) are scaled by the square of the transformer turns ratio. Having a larger value of magnetizing inductance significantly reduces the amount of current drawn by the active filter supply as it reduces the magnetizing current drawn. Also, having a larger value of primary leakage inductance (within a certain range) was shown to provide greater filtering of the high

frequency active filter PWM voltage. The added filter capacitor and the combination of primary and secondary-side leakage inductances function as an LC filter whose corner frequency was chosen to be between the switching frequency of the inverter and that of the active filter. This allows a greater attenuation of the added high-frequency active filter PWM voltage. This circuit was proven in simulation to equivalently represent the full three-phase active filter circuit.

3.3 H-bridge PWM strategy

Mentioned above, an advantage of this proposed active filter is that it is controlled using direct knowledge of the status of the common-mode voltage based on the control of the inverter. More specifically, since the sum of the number of switches that are driven high determines the voltage level that the common-mode voltage assumes at any point in time (refer to Table 2.1), the active filter voltage needed to compensate the common-mode voltage can be controlled without any voltage sensing circuitry and resulting time delay. The inverter is controlled via open-loop logic programmed into an FPGA platform, and additional logic is combined with the original inverter logic to sum the gate pulses going to the switches of the inverter.

The size of the CM transformer can be reduced by preventing the active filter from generating output voltages at low frequencies where there is no concern of sizable shaft voltages or CM bearing currents. Although this is not a consideration in sine-triangle PWM, in carrier-based SVPWM a triangular wave (which is the mid of the reference signals) is added to the duty ratios of each phase in order to fully utilize the DC bus voltage [11]. This triangular wave creates lower-harmonic components (odd triplen harmonics of the fundamental load voltage) in the resulting common-mode voltage produced by the inverter. These frequency components are sufficiently low that the active filter does not need to compensate for them and therefore can be safely removed from the active filter's output voltage as a means of reducing the transformer size [18]. As mentioned before, previous techniques to remove this low frequency voltage have relied on passive LC circuit components, such as in [18] where a series capacitor is added on the active filter side of the CM transformer to form a high-pass filter with the transformer inductances. In contrast to using passive circuit components, the method proposed in this

paper removes the low-order harmonics within the digital PWM algorithm of the active filter. This means that the H-bridge output voltage only consists of the desired high frequency components and no passive filter circuitry is required.

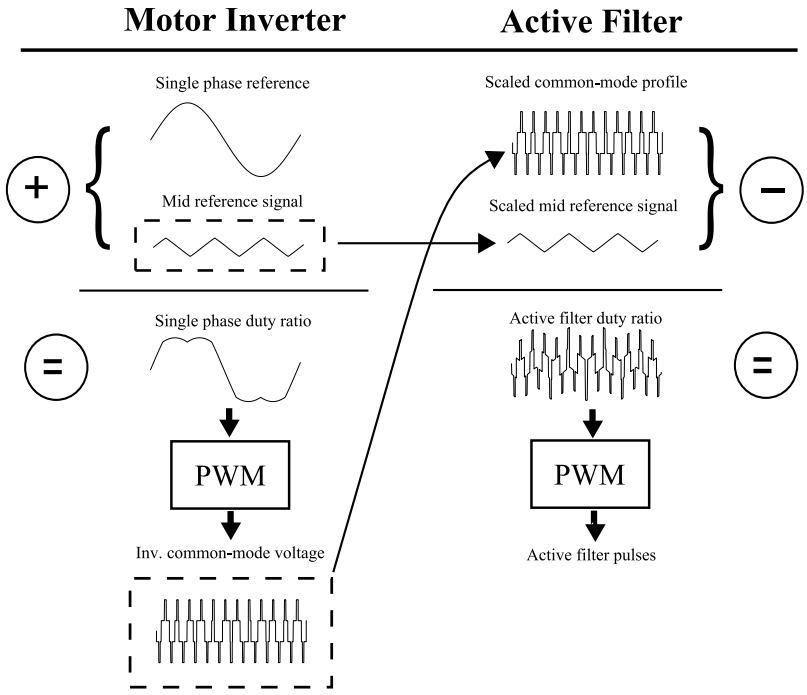

Figure 3.4: Control strategy used to generate duty ratio for the active filter

The final PWM algorithm used for the H-bridge is now described and an overview is shown in Fig. 3.4. The active filter utilizes the switching pulses of the VSI to construct the reference output voltage for the H-Bridge (this is effectively a scaled common-mode voltage profile, with the low frequency components still present). The SVPWM triangle waveform ("Mid. reference signal" in Fig. 3.4, source of the low-order CM voltage) is then subtracted from the reference output voltage for the active filter to remove the lower-order harmonic content. Finally, this new reference voltage is then scaled according to the CM transformer turns ratio to obtain a duty ratio for the H-bridge ("Filter duty ratio" in Fig 3.4). This duty ratio is then compared to a carrier wave to produce the PWM pulses sent to the H-bridge. The results of this technique in simulation are depicted in Fig. 3.5, which shows that the low frequency content of the

original CM voltage has been effectively eliminated from the filter reference voltage.

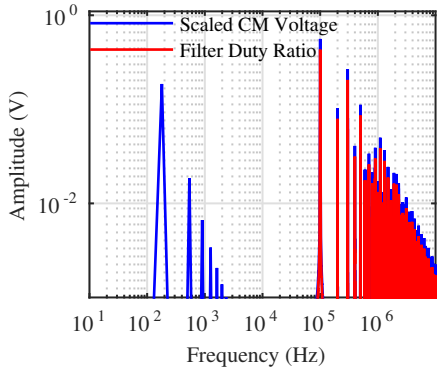

Figure 3.5: Filter duty ratio spectra after removal of lower order harmonics

Chapter 4

Simulation

4.1 Simulation Procedure

Simulations for the full three-phase model of the proposed active filter were performed in MATLAB/Simulink. The VSI used in simulation consisted of ideal MOSFET switches and a 400V DC bus. Dead-times of 1 percent of the inverter switching time period were added externally to the pulses controlling the inverter. The H-bridge active filter consisted of ideal MOSFET switches and a 26V DC bus. The four-winding step-up common-mode transformer used to inject the compensating voltage consisted of an ideal transformer block with a turns ratio of 1:10:10:10. Primary and secondary leakage inductance and winding resistance as well as magnetizing inductance were added appropriately as additional components. The switching frequency of the VSI in simulation was chosen to be 100kHz to align with the SiC inverter used in previous hardware experimentation. A switching frequency of 2MHz was used for the active filter, as this was found to be a favorable lower limit relative to the CM voltage switching frequency.

4.2 Simulation Results

The CM voltage seen at the motor terminals (V_{mot}) was measured with and without the active filter. Fig. 4.1 shows the transient comparison of V_{mot} before and after filtering. V_{mot} without the active filter (second from top) is the original CM voltage at the output of the inverter caused by SVPWM and switches at the inverter switching frequency. The

third from the top waveform of Fig. 4.1 shows V_{mot} after the addition of the active filter with and without the passive filter. It can be seen that the CM voltage at the motor terminals has been drastically reduced. The filtered V_{mot} waveform has a triangular shape due to the removal of the lower-order harmonics from the compensating voltage in the previously described PWM logic of the active filter. As noted earlier, this slow-varying voltage is not harmful to the motor and its bearings. To demonstrate the importance of preventing the active filter from canceling the low frequency CM voltage, the bottom of Fig. 4.1 shows the substantial increase of the transformer's magnetizing current when active filter also acts to cancel the low frequency components of the CM voltage.

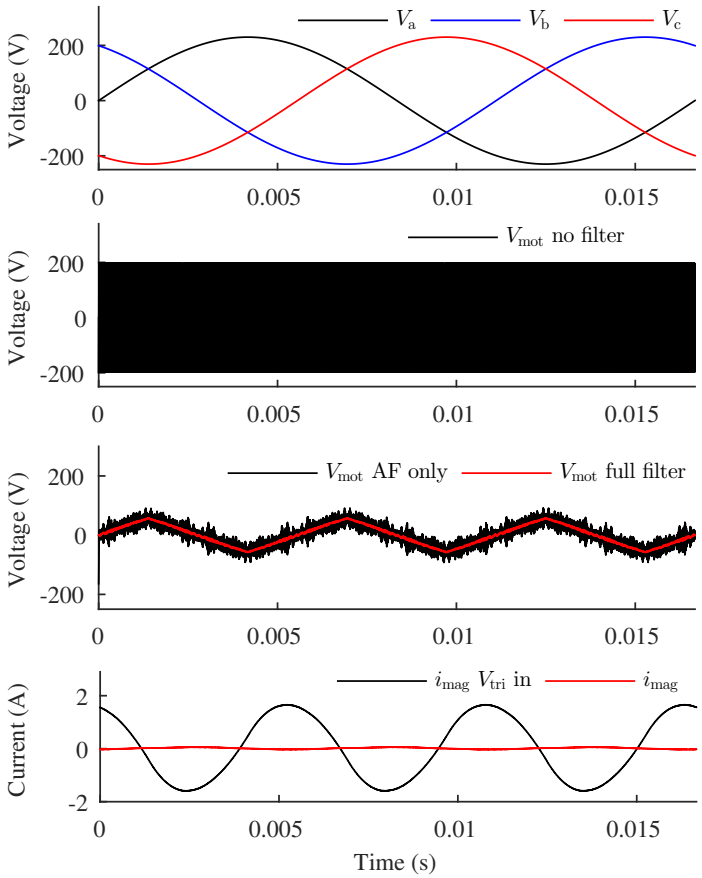

Figure 4.1: Simulation results - transient waveforms

Shown in the middle plot of Fig. 4.2 are the spectra of V_{mot} without any filtering, with solely active filtering, and with the full active filter (including the passive filter). These plots show that the full active filter successfully attenuates the primary 100kHz switching component of the CM voltage, as well as the higher frequency components introduced by the active filter. The clear difference between the spectra plot of V_{mot} with active filtering only and the full active filter shows the advantage of adding the passive components to remove the presence of higher frequency noise. In order to confirm that the active filter has a significant impact, a plot of spectra comparing V_{mot} with no filtering and with only passive filter components is shown in the bottom of Fig. 4.2. There is a negligible effect on the main 100kHz component of V_{mot} with only passive filtering compared to the results with the full active filter in place. Once again in these plots, the lower order harmonics of V_{mot} remain and are not filtered due to the removal of lower-order harmonics in the compensating voltage.

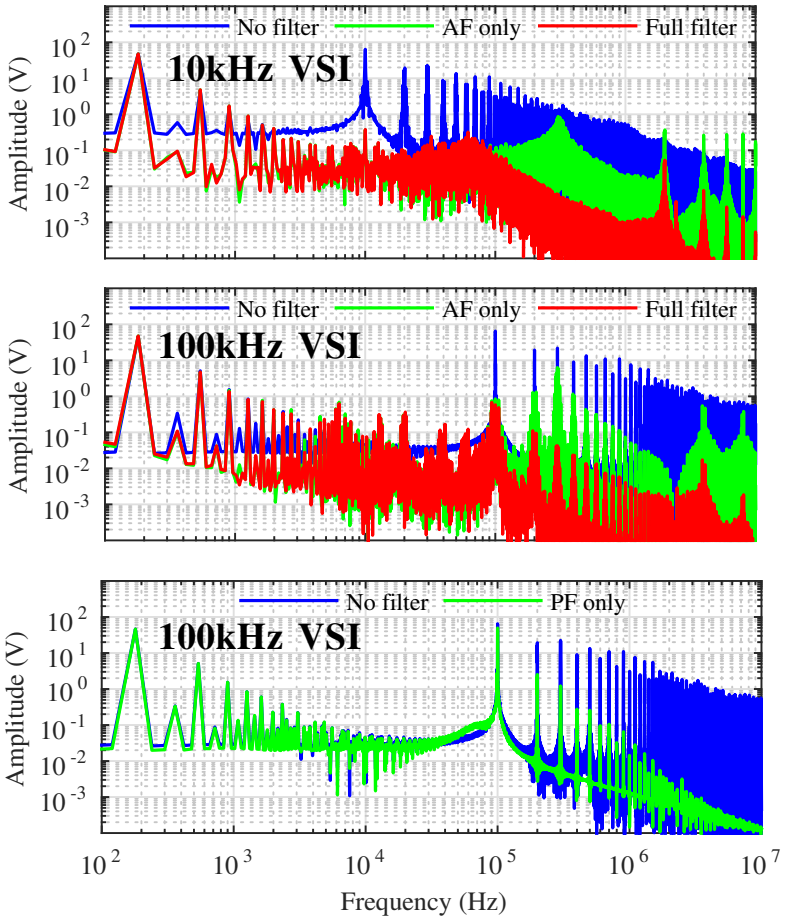

Figure 4.2: Simulation results - spectrum waveforms

Also shown in the top plot of Fig. 4.2 is the performance of the active filter when the switching frequency of the inverter is set at 10kHz (1 μs of dead time and 1 MHz H-bridge switching frequency). This is done to demonstrate the feasibility of the active filter in more commonly found Si-based inverters, which switch at relatively lower frequencies. Comparing once again V_{mot} without filtering, and with the full active filter, the spectra plots show sufficient attenuation of the CM voltage produced by the inverter.

Chapter 5

Hardware Implementation

5.1 Experimental Setup

The experimental setup is shown below in Fig. 5.1. It consists of the H-bridge active filter tied to the three phases of the original SiC inverter via a common-mode transformer. The inverter drives a 1-hp induction motor coupled to a DC motor acting as a load. As previously mentioned, the motor drive is a three-phase, two-level inverter built with SiC MOSFETs (ROHM SCH2080KEC), where each phase leg is a half-bridge consisting of two SiC switches. The active filter H-bridge was built utilizing two GaN half-bridge development boards from EPC (EPC9030). Each board contains two GaN MOSFETs rated at 100V and 2.7A in a half-bridge topology with onboard gate drives. These boards were chosen due to their ability to switch in the 1-10MHz frequency range and low relative power need. The common-mode transformer was built using a toroidal core and was hand wound in the lab. In order to achieve the desired 1:10:10:10 step-up turns ratio, 6 turns were added for the primary winding, and 60 turns were added for each of the three secondary windings. Not pictured, additional series inductance was added to the active filter side of the transformer, as it was shown in simulation to provide additional filtering of the high frequency components of the active filter voltage. A Nexys 4 DDR Artix-7 FPGA supplied the gate pulses to both the inverter and the active filter H-bridge. The embedded control for this system was developed in Verilog using Xilinx ISE design suite. Finally, a grounding braid is connected from the shell of the induction motor to the grounded negative of the DC bus voltage. This provides a

path for common-mode currents to flow in the system.

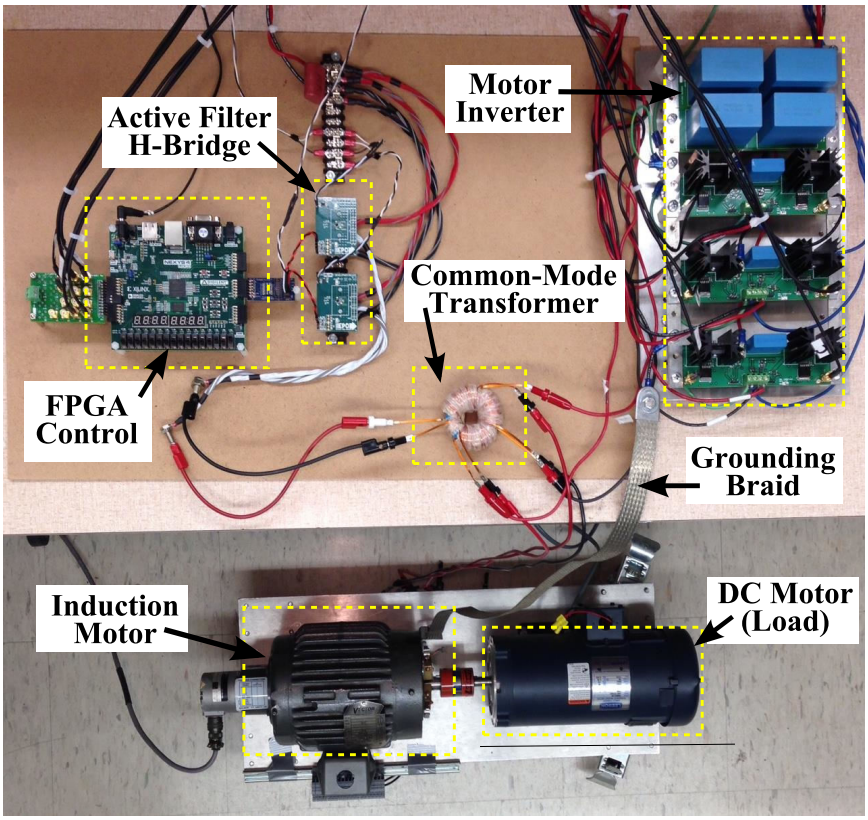

Figure 5.1: Active filter hardware setup

5.2 Experimental Procedure

Experimental results were obtained for an operating point of 10kHz inverter switching frequency, and 500kHz active filter switching frequency at an inverter DC bus voltage of 100V. The fundamental frequency of the inverter was kept at 30Hz and dead times for the inverter were set to $100ns$ This operating point was chosen for the reason that it provided the clearest example of filtering as a proof of concept of this hardware prototype. Analysis of the transformer being used showed an unwanted resonance at frequencies above 1MHz, so the active filter was operated below this frequency. This in turn limited the inverter switching frequency. Future work will be done to obtain

results at the operating points of the simulation results in Chapter 4.

In order to observe the effect of the active filter, the common-mode voltage seen at the motor terminals (V_{mot}), the common-mode current (i_{CM}), and the shaft voltage (V_{shaft}) were studied for three cases: 1) with no added components in the common-mode path, 2) with solely the active filter voltage being supplied, and 3) with the active filter and added primary-side series inductance for filtering purposes.

V_{mot} was obtained by measuring each of the three phase voltages at the input terminals of the motor with respect to ground and performing a math operation in the oscilloscope to add and scale the resulting waveforms. The phase voltages were measured with differential voltage probes. The common-mode current, i_{CM}, was measured at the input of the motor by passing all three phase through a high-bandwidth Pearson Model 6585 current transformer. The shaft voltage, V_{shaft}, was observed via a differential voltage probe connected between a brush contacting the rotor shaft and the grounding braid.

5.3 Hardware Results and Analysis

5.3.1 CMV Reduction at Motor Input Terminals

As mentioned above, the common-mode voltage seen at the input terminals of the motor, referred to as V_{mot}, was measured without any filtering hardware added, and after the addition of the active filter with and without additional passive filtering hardware (series inductance in the active filter path). These results are shown below in Figures 5.2 and 5.3. Fig. 5.2 shows the filtering of V_{mot} on the timescale of the 30Hz fundamental frequency of the inverter. The top graph is the original V_{mot} waveform which has a peak-to-peak voltage of the $100V$ DC bus voltage. The middle graph shows V_{mot} now with the $500kHz$ active filter voltage being added, but without being filtered fully. The bottom waveform of Fig. 5.2 shows the full effect of the active filter and additional inductance to remove some of the higher frequency switching. It is clear in both the middle and bottom graphs that the lower frequency (third harmonic and its multiples) component of the common-mode voltage has been left uncompensated for as intended since it appears in the final filtered waveforms.

To get a clearer picture of the filtering action, these same waveforms were observed

on a timescale of the inverter switching frequency (Fig. 5.3). The top graph shows the distinct four-level waveform expected of the original V_{mot} without any filtering. In the middle waveform, the addition of the 500kHz active filter voltage is evident. There are still clear transitions based on the level of the common-mode voltage, but it can be seen that the addition of the PWM active filter voltage causes the resulting V_{mot} to approximately average to zero. Finally, the bottom graph shows the effect of the full active filter. The high frequency component in the previous waveforms is almost completely attenuated by the addition of series inductance in the active filter path.

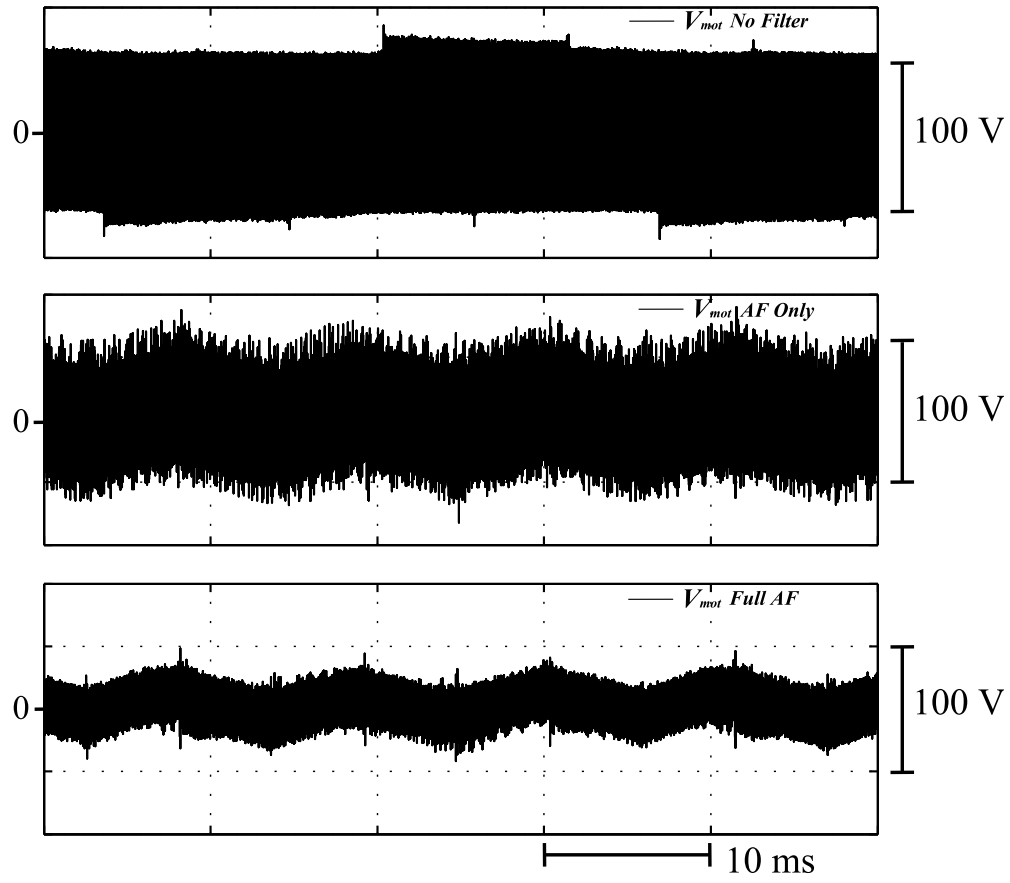

Figure 5.2: V_{mot} waveforms on fundamental timescale

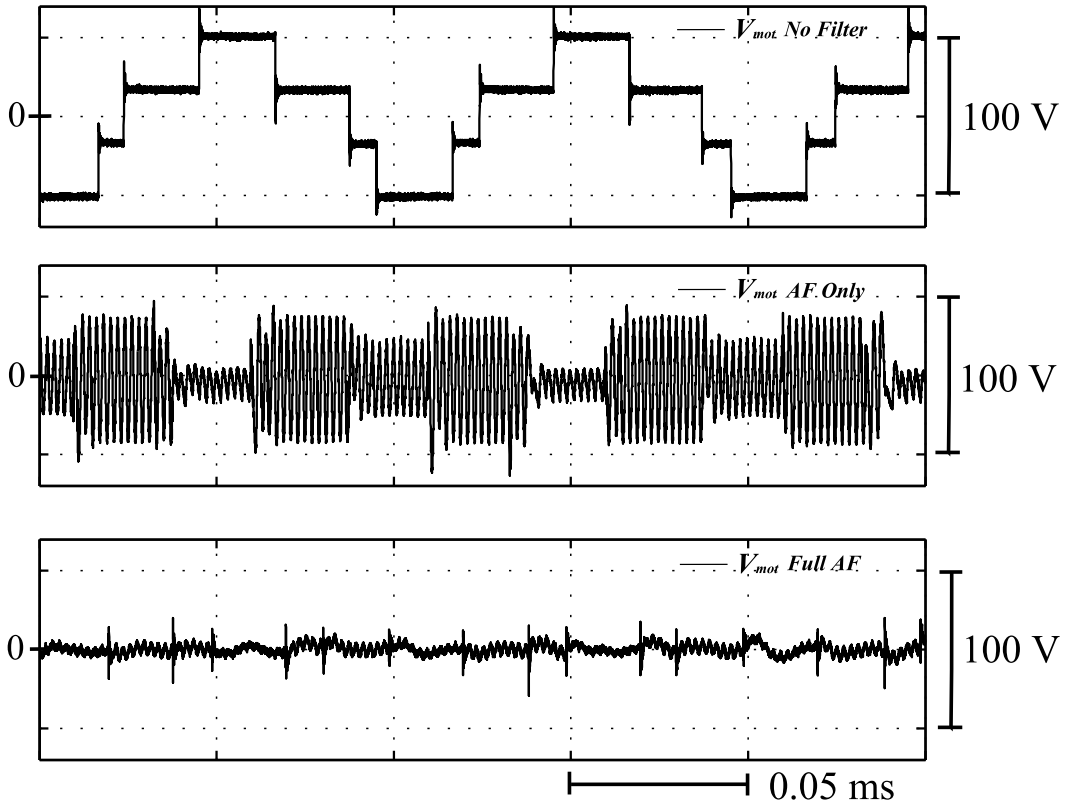

Figure 5.3: V_{mot} waveforms on inverter switching timescale

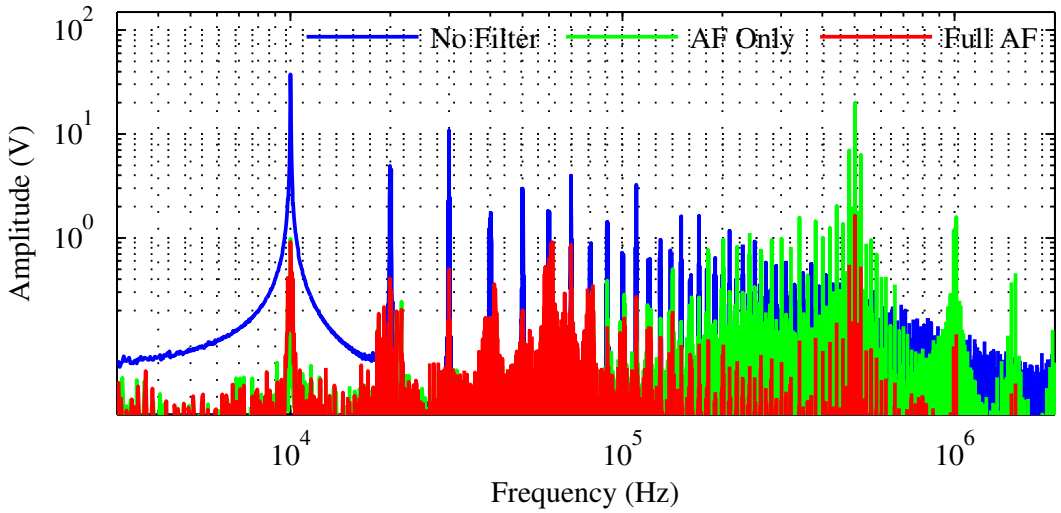

Figure 5.4: V_{mot} spectra analysis

In order to get a measure of the performance of the active filter, spectra analysis of the above three cases was conducted. Seen in Fig. 5.4, the magnitude of the 10kHz component of V_{mot} is reduced by a factor of approximately 13 when the full active filter is implemented. There are also significant reductions in the higher order harmonics of the common-mode voltage. The presence of the added 500kHz active filter voltage can be seen clearly in the case where there are no added passive components. This 500kHz component and it's higher order harmonics are reduced with the addition of the added series inductance in the active filter path.

5.3.2 CM Current Reduction

Similar results to section 5.3.1 were taken to show the effect of the active filter on the common-mode current, i_{CM}. Plots of i_{CM} were obtained for the cases of no filter, active filter only, and full active filter on the fundamental timescale as well as the inverter switching timescale (Figures 5.5 and 5.6 respectively). A clear reduction in the magnitude of the peaks magnitude of the current spikes caused by the step transitions of the common-mode voltage can be seen by comparing the top and bottom waveforms of Fig. 5.6. This reduction is also evident in the spectra analysis of Fig. 5.7, where the 10kHz component and its multiples are significantly reduced after the addition of the

active filter. Also visible in this plot is the unwanted effect of adding the high frequency 500kHz active filter PWM voltage. The peaks at 500kHz and its higher orders are reduced by the addition of the added series inductance, but additional reduction is desired.

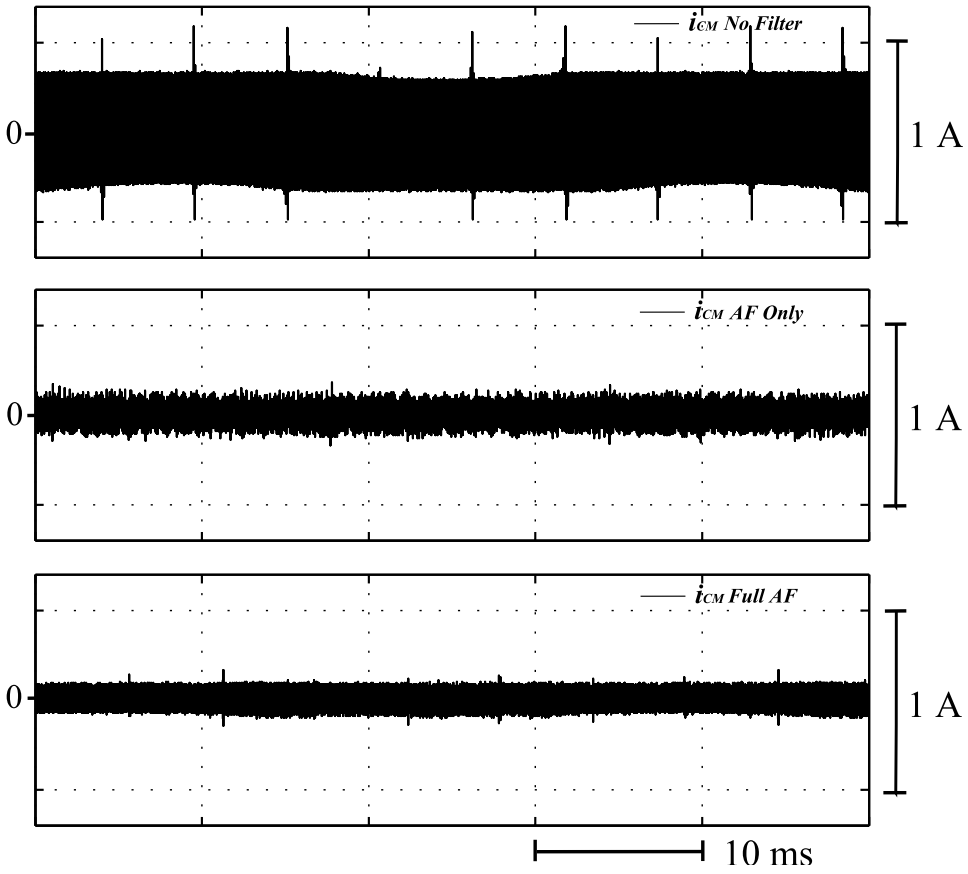

Figure 5.5: i_{cm} waveforms on fundamental timescale

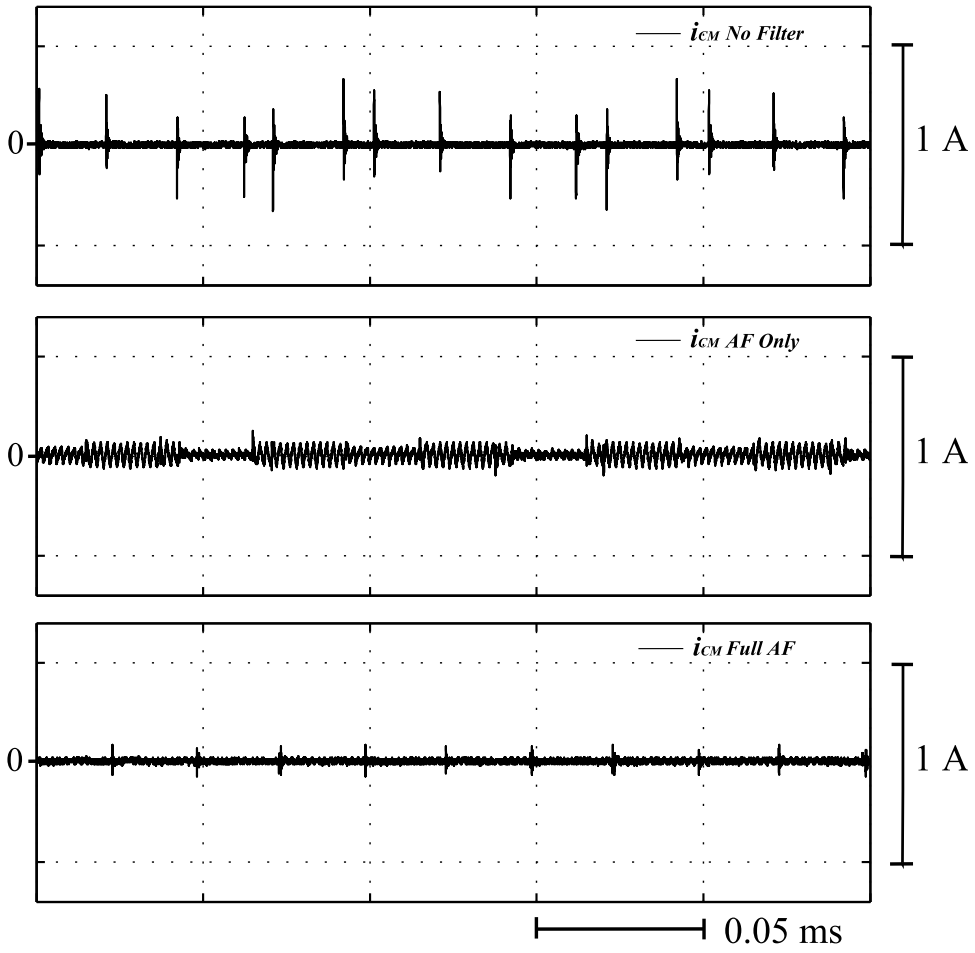

Figure 5.6: i_{cm} waveforms on inverter switching timescale

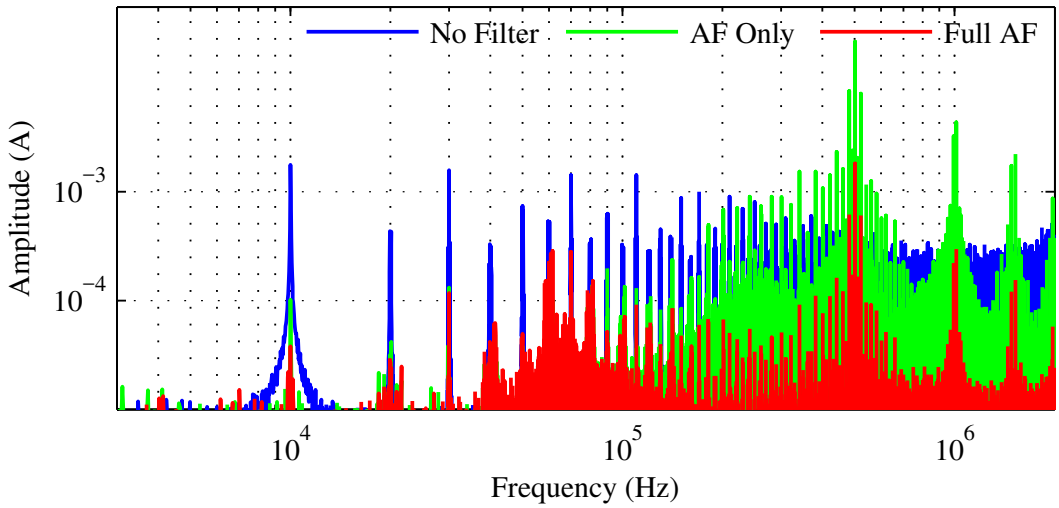

Figure 5.7: i_{cm} spectra analysis

5.3.3 Shaft Voltage Reduction

Finally, verification is given that the voltage developed at the shaft of the motor, V_{shaft}, is reduced with the addition of the active filter. Based on the simplified understanding of the induction motor from previous research, it should follow that with the reduction of the common-mode voltage at the input terminals of the motor (V_{mot}) comes the reduction of V_{shaft}. This is shown visually in the waveforms of Figures 5.8 and 5.9, and verified in the spectra analysis of Fig. 5.10.

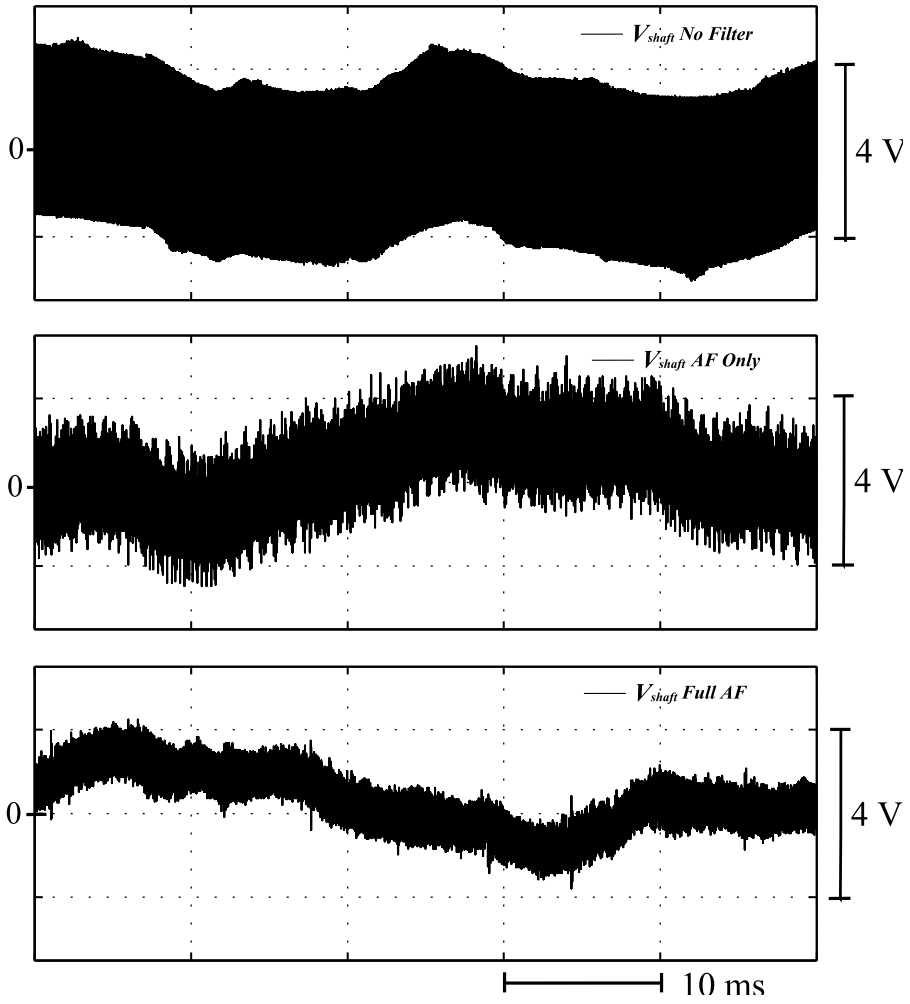

Figure 5.8: V_{shaft} waveforms on fundamental timescale

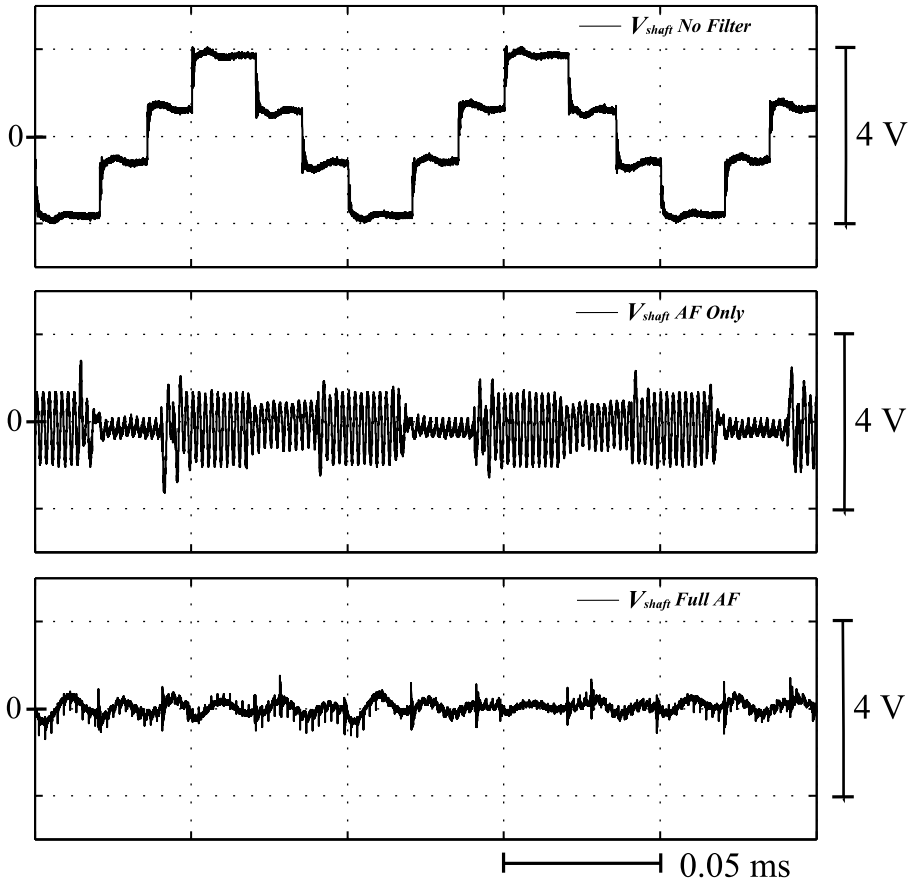

Figure 5.9: V_{shaft} waveforms on inverter switching timescale

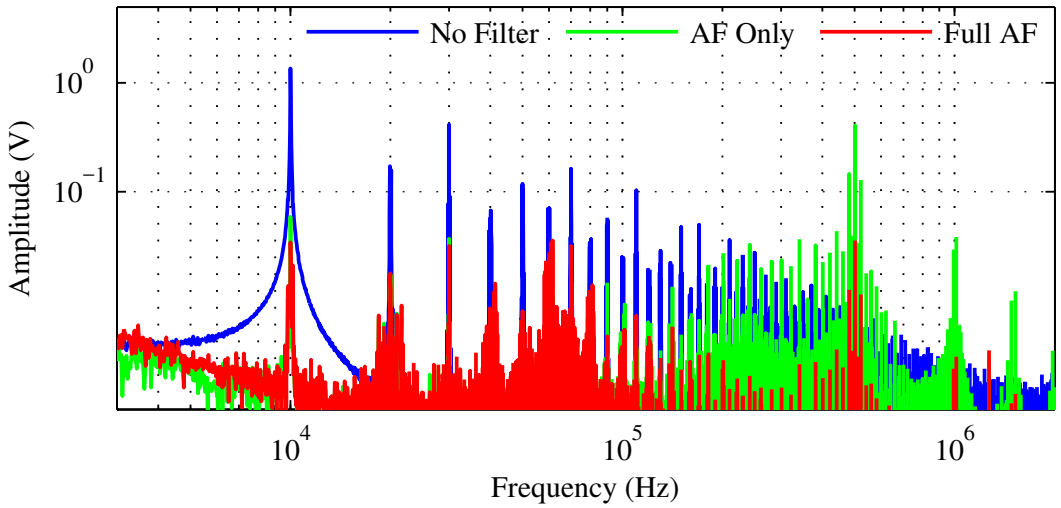

Figure 5.10: V_{shaft} spectra analysis

5.4 Additional Investigation Points

5.4.1 Effect of CM Transformer Only

A point was made in the simulation results to show that only having the common-mode transformer added (no active filter voltage applied) did not sufficiently act to suppress the common-mode voltage. Shown below in Fig. 5.11 is a comparison of screenshots of the shaft voltage in the case when no filtering hardware was added (top), and when just the common-mode transformer was added (bottom). This comparison shows that the added inductance from the transformer acts to smooth out the CM voltage profile, but does not reduce the 10kHz fundamental component at the switching frequency of the inverter.

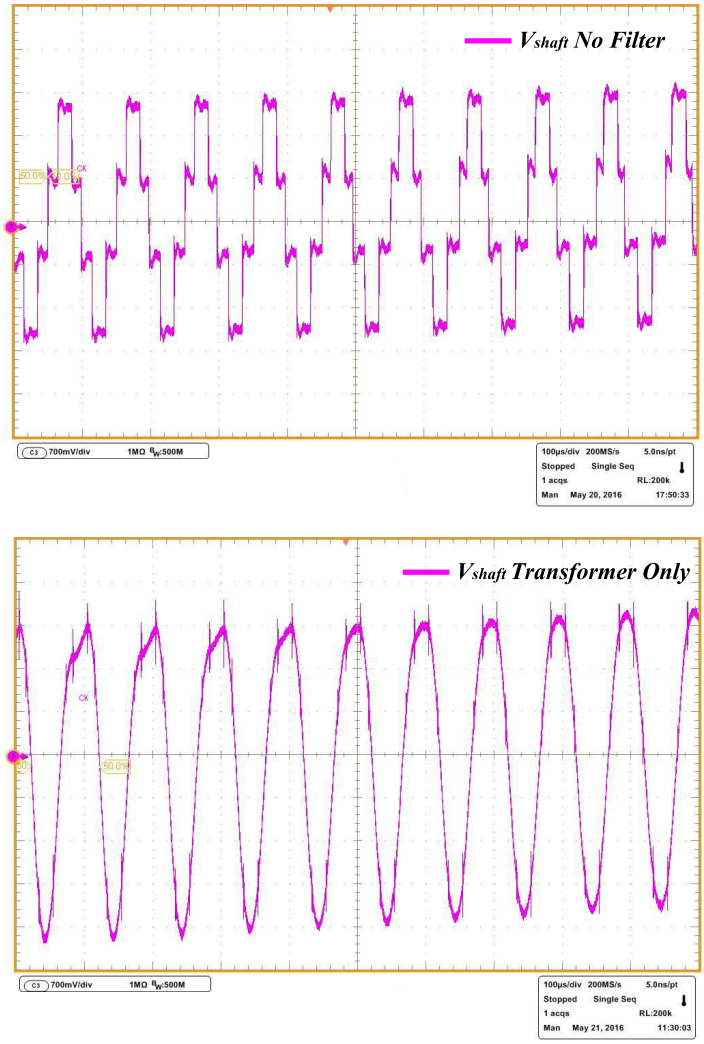

Figure 5.11: V_{shaft} comparison with and without CM transformer

5.4.2 Active Filter Voltage Waveforms

In order to get a picture of the voltage being supplied by the active filter, the voltage across the primary winding of the common-mode transformer during operation was measured. Figure 5.12 shows this voltage (labeled V_{AF}) and also the current being drawn by the active filter for both when only the active filter voltage is supplied (top) and after the addition of primary-side series inductance (bottom). You can see from

the top screenshot that there are four levels that are somewhat defined, but much of the PWM voltage remains. After the addition of the series inductance, the four levels become much more clear and resemble a suitable compensating voltage to be supplied to the three phases of the inverter. There is also a significant decrease in the output current ripple of the active filter when the additional inductance is present.

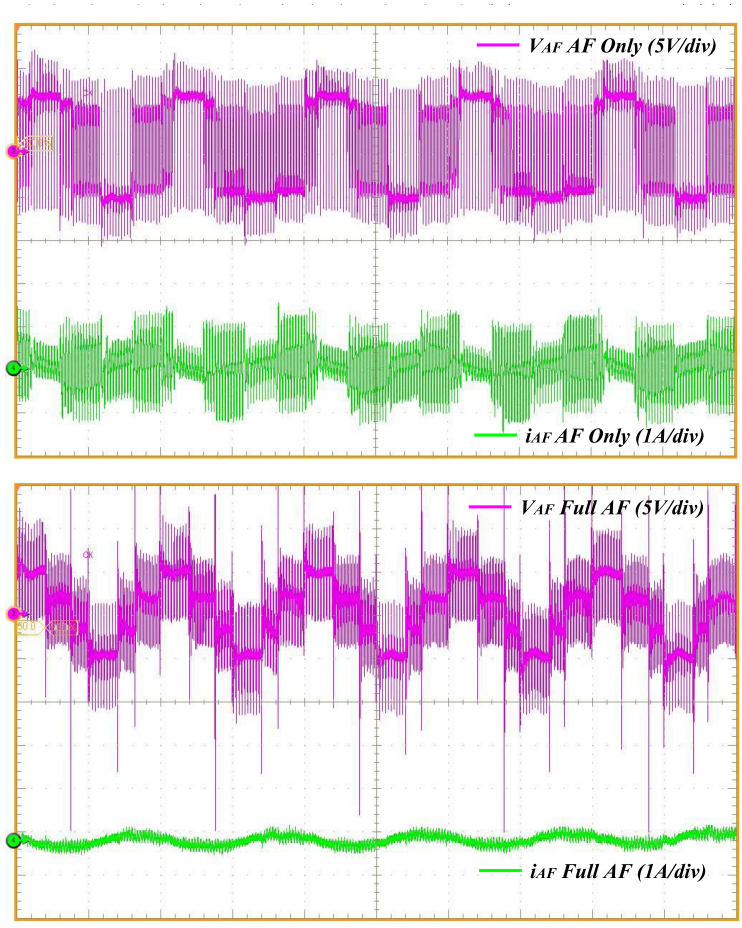

Figure 5.12: V_{AF} and i_{AF} waveforms during active filter operation

Chapter 6

Conclusion and Future Work

Previous studies have shown the harmful effects of CM voltage and resulting bearing currents and EMI in SVPWM inverters. Mitigation of CM voltage is essential to maximizing the motor lifetime, and is even more important with the recent emergence of WBG devices in motor drives.

This thesis presents a new active filter device for the suppression of common-mode voltage in SVPWM electric motor drives. This new filter has advantages over previous mitigation techniques in a trade-off of performance versus size and amount of required hardware. The proposed active filtering method consists of a 2-level PWM H-bridge inverter supplying a compensating voltage via a four-winding CM transformer which will be shown to effectively suppress CM voltage at the motor terminals. Transient and spectra results in MATLAB/Simulink simulation before and after the addition of the active filter demonstrate a significant reduction in the drive system's CM voltage. A hardware prototype was built and experimental results act as a proof of concept of the proposed active filter. Transient results show a clear reduction in the magnitude of the common-mode voltage seen at the terminals of the induction motor and also in the resulting shaft voltage. Common-mode currents are also shown to reduce with the addition of the active filter to the motor drive system.

6.1 Future Work

As mentioned previously in the experimental procedure section, the hardware results for this paper are for an operating point which allows the clearest example of the filtering possibilities of this new proposed filter. Some adjustments to the hardware setup need to occur in order for results to be obtained at operating points that will allow for the comprehensive comparison of the performance of this method to other previous methods. These additional immediate steps as well other future work topics for this research project are outlined below:

- Resolve unwanted resonance issues with the common-mode transformer at frequencies above 1MHz by using a more suitable core and optimized winding configuration.
- Implement the full active filter as described in the proposed filter section of this paper and verified in simulation by adding the wye-connected filter capacitor to the hardware prototype.
- Obtain results for the operating points verified in simulation and also for those reported in previous experimentation in order to accurately compare this filter's relative performance.
- Perform a full analysis of the space and device requirements of this active filter compared to other common-mode mitigation techniques. A cost analysis would follow.

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